NOVEL PASSIVE NEGATIVE AND POSITIVE CLAMPER CIRCUITS DESIGN FOR ELECTRONIC SYSTEMS

Martin C. Eze, Hyginus U. Eze, Nnachebem O. Chidebelu, Samuel A. Ugwu, Jonathan I. Odo, Josiah I. Odi

Abstract- In this paper, models for negative and positive clamper circuits were developed. The models developed were simulated and data collected. Simulation results obtained showed that series capacitance needed to design negative clamper circuit was directly proportional to the duty cycle and period of the input signal. Considering the positive clamper circuit, the series capacitance is inversely proportional to the duty cycle and directly proportional to the period of the input signal. Looking at the parallel resistance, the parallel resistance needed to design negative clamper circuit is inversely proportional to the duty cycle but for positive clamper circuit, the parallel resistance is directly proportional to the duty cycle of the input signal. The models were also validated using Simscape and the results agreed. The models developed were simulated using Matrix Laboratory (MatLab).

Keywords:Matrix Laboratory, Negative clamper circuit, parallel resistance,positive clamper circuit, series capacitance, Simscape

1.0 Introduction

Clamping is a technique used by engineers to limit the input current to a certain value to avoid damaging of the circuit[1]. Clamp Circuit is a special type of circuit that is used to limit or clamp the output voltage to a specific range using diodes, capacitors and resistors. It consists of a diode, which allows the circuit to conduct only one direction and does not allow the current to flow in reverse direction, acapacitor which clamps the voltage and the load resistor which determines the capacitor discharge period[2]. The capacitor was connected to the gate input electrode of the device for clamping function. Time constants for charging and discharging modes must be taken into account with the operation switching frequency when determining the capacitance value[3].

Normally positive and negative clamper circuits exist. The positive clamper circuit clamps the input signal to the positive voltage axis without deforming the original signal. On the other hand, the negative clamper circuit clamps the input signal to the negative voltage axis without deforming the original signal. In all clamper circuits, the diode is connected in parallel to the load.

A lot of work has been done on the design of electronic clamper circuits [4][2][3][5]. In [4], an active electronic clamper circuit was designed for balancing the dynamic voltage during thebreakdown.In [2], clamped circuit is designed to limit overload current in theresonant circuit. In [3], a clamper circuit was designed using AlGaN/GaN Heterojunction Field-Effect Transistor (HFET) with Schottky gate structure. The Schottky gate of an HFET serves as a clamping diode.Switching frequency of 10 kHz with a 50% duty cycle and 5nF capacitance value was used in [3]. In [5], local replicated network (LRN) clamper circuit was developed.

In this paper, models for passive negative and positive clamper circuits were proposed. The validation of the developed models was carried out using Simscape.

2.0.Modelling of passive clamper circuits

A novel model for passive clamper circuit is developed in this paper. In the paper, both positive and negative clamper circuits are considered.

2.1.Negative Clamper Circuit Design

Figure 1 shows the diagram of a passive negative clamper circuit. Vc is the voltage across the capacitor at any time instant, R is the value of theresistor in parallel to the load. Finally, D represents the diode. In this paper, silicon diode was assumed. The models for negative clamper circuits are derived in sections 2.1.1 and 2.1.2. Section 2.1.1 models the charging mode while section 2.1.2 models the discharge mode.

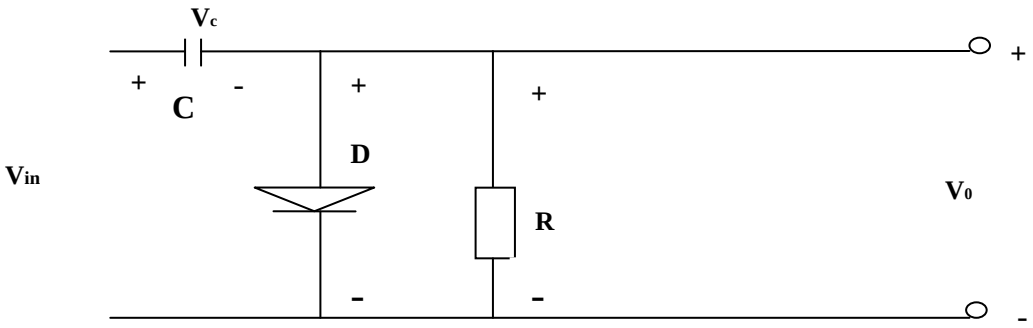

Figure 1:Negative Clamper Circuit

2.1.1.Capacitor Charging Cycle (Positive Cycle)

During the capacitor charging cycle of negative clamper circuit, the circuit is simplified as shown in Figure 2. Applying Kirchhoff's law to Figure 2, V_0 and Vc are as given in equations (1) and (2) respectively.

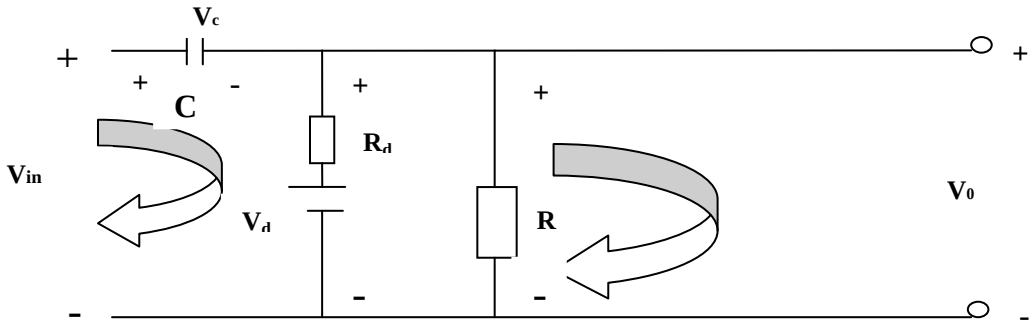

Figure 2: Charging/Positive Cycle.

$$V_0 = V_d \qquad (1)$$

$$\boldsymbol{V_C = (V_{in}^{+} - V_d)\left(1 - e\frac{-t_c}{R_d C}\right)} \qquad (\mathbf{2})$$

In equations (1) and (2), V_d is the diode threshold voltage, V_0 is the clamper circuit output voltage, Vc is the capacitor voltage, D is the duty cycle of the input voltage, T is the period of the input voltage, R_d is the forward resistance of the diode and C is the capacitance of the capacitor. V_{in}^{+} is the positive amplitude of the input voltage and $t_c$is the charging time, with range $0 \leq t_c \leq DT$. The expression for the capacitor value is given inequation (3).

$$C \leq \frac{DT}{50R_d} \qquad (3)$$

2.1.2 Capacitor Discharging Cycle (Negative Cycle)

During the capacitor discharging cycle of negative clamper circuitthe circuit is simplified as shown in Figure 3. Applying Kirchhoff's law to Figure 3, $V_0$is as given in equation (4) where V_{in}^{-} is the negative amplitude of the input voltage and Vcm is the maximum voltage across the capacitor.

$$\boldsymbol{V_o = -\left(V_{in}^{-} + V_{cm}e^{\frac{-(t_d - DT)}{RC}}\right)} \qquad (\mathbf{4})$$

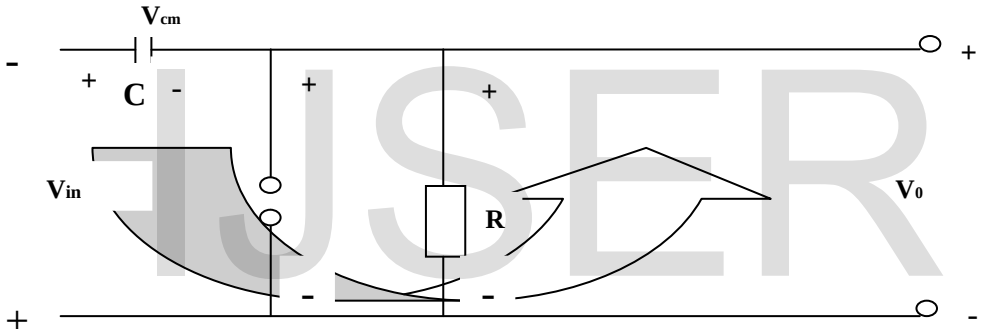

Figure 3: Discharge/Negative Cycle

At the end of charging period, the capacitor is fully charged and the expression for capacitor voltage (Vcm) is given as in (5).

$$\boldsymbol{V_{cm} = (V_{in}^{+} - V_d)\left(1 - e\frac{-DT}{R_d C}\right)} \qquad (\mathbf{5})$$

Substituting equation (5) in equation (4), equation (6) is obtained.

$$V_o = -\left(\boldsymbol{V_{in}^{-}} + (\boldsymbol{V_{in}^{+}} - V_d)\left(1 - e^{\frac{-DT}{R_d C}}\right)\boldsymbol{e^{\frac{-(t_d - DT)}{RC}}}\right) \qquad (6)$$

In equations (4) and (6) capacitor discharge time, t_d is valid for$DT \leq t_d \leq T$ and expression for R is given in equation (7).

$$R \geq 10000\left(\frac{1-D}{D}\right)R_d \qquad (7)$$

2.2.Positive Clamper Circuit Design

Figure 4 shows the diagram of a passive positive clamper circuit. Vc is the voltage across the capacitor at any time instant, R is the value of theresistor in parallel to the load. Finally, D represents the diode. In this paper, silicon diode was assumed. The models for negative clamper circuits are derived in sections 3.1 and 3.2. Section 3.1 models the charging mode while section 3.2 models the discharge mode.

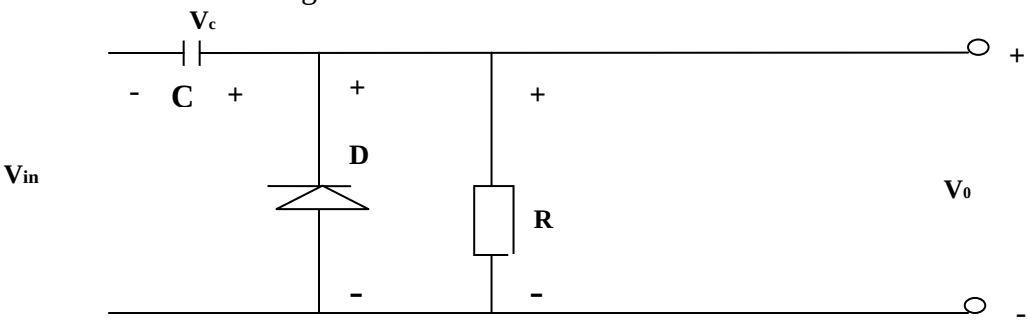

Figure 4: Positive Clamper Circuit

2.2.1. Capacitor Charging (Negative cycle)

During the capacitor charging cycle of positive clamper circuit,the circuit is simplified as shown in Figure 5. Applying Kirchhoff's law to Figure 5, V_0 and Vc are as given in equations (8) and (9) respectively.

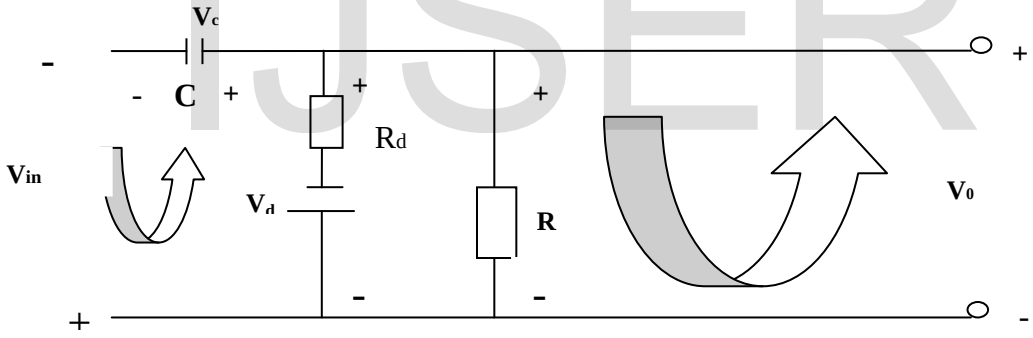

Figure 5: Capacitor Charging or Negative Cycle

$$V_o = -V_d \qquad (8)$$

$$V_c = (V_{in}^{-} - V\mathrm{d})\left(1 - e\frac{-t_c}{R_d C}\right) \qquad (9)$$

The capacitor charging time $t_c$is valid for $0 \leq t_c \leq (1-D)T$ and expression for capacitor value is given in (10).

$$C \leq \frac{(1-D)T}{50R_d} \qquad (10)$$

2.2.2. Capacitor Discharging (Positive cycle)

During the capacitor discharging cycle of positive clamper circuit,the circuit is simplified as shown in Figure 6. Applying Kirchhoff's law to Figure 6, $V_0$is as given in equations (11) whereV_{in}^- is the negative amplitude of the input voltage and Vcm is the maximum voltage across the capacitor.

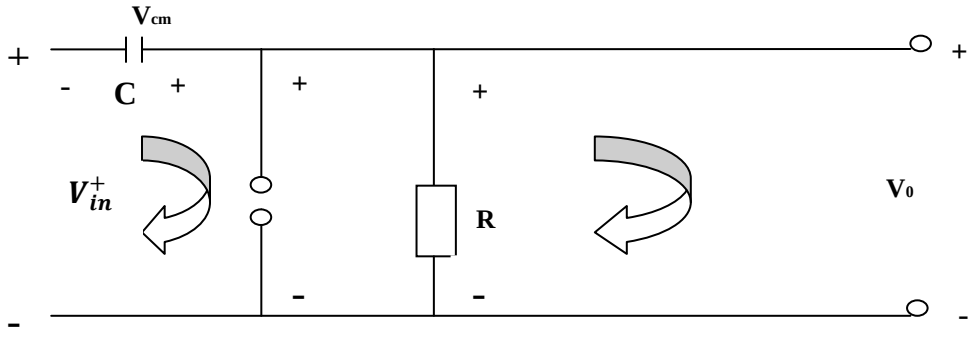

Figure 6: Discharging/positive cycle

$$V_0 = V_{in}^+ + V_{cm}\, e^{-\left(\frac{(t_d-(1-D)T)}{RC}\right)} \qquad (11)$$

At the beginning of discharge cycle, the capacitor is fully charged and the expression for the capacitor voltage (Vcm) is given by (12).

$$V_{cm} = (V_{in}^- - V\mathrm{d})\left(1 - e\frac{-(1-D)T}{R_d C}\right) \qquad (12)$$

Substituting equation (12) in equation (11), equation (13) is obtained.

$$V_0 = V_{in}^+ + (V_{in}^- - V_d)\left(1 - e\frac{-(1-D)T}{R_d C}\right)\, e\frac{-(t_d-(1-D)T)}{RC} \qquad (13)$$

The capacitor discharge time, $t_d$in equations (7) and (9)isvalid for $(1-D)T \le t_d \le T$ and expression for R is given in equation (14).

$$R \ge 10000\left(\frac{D}{1-D}\right)R_d \qquad (14)$$

3.0.Results and Discussion

The results presented in Tables 1-11 were generated by simulatingequations (1)–(14) using MatLab. The diode in the circuits was assumed to be silicon diode internal resistance of 27Ω and reverse voltage of 0.7V.

The results in Table 1 were obtained from equations (3) and (10). Table 1 showed how the capacitance value (C) varied with the duty cycle for both positive and negative clamper circuits for100kHz frequency input signal. The table showed that for negative clamper circuit, the capacitance is directly proportional to the duty cycle while for positive clamper circuit; the capacitance is inversely proportional to the duty cycle of the input signal.

Table 1: Effect of input voltage duty cycle on the capacitor value for positive and negative clamper circuit

Clamper Circuit Type	Input voltage duty cycle (%) at 100kHz								
	10.00	20.00	30.00	40.00	50.00	60.00	70.00	80.00	90.00
	Capacitor Value (nF)								
Negative	0.74	1.48	2.22	2.96	3.70	4.44	5.19	5.93	6.67
Positive	6.67	5.93	5.19	4.44	3.70	2.96	2.22	1.48	0.74

The result in Table 1 was clearly presented in Figure 7. The figure also showed that capacitance for negative clamper was directly proportional while the capacitance of positive clamper was inversely proportional to the input signal duty cycle.

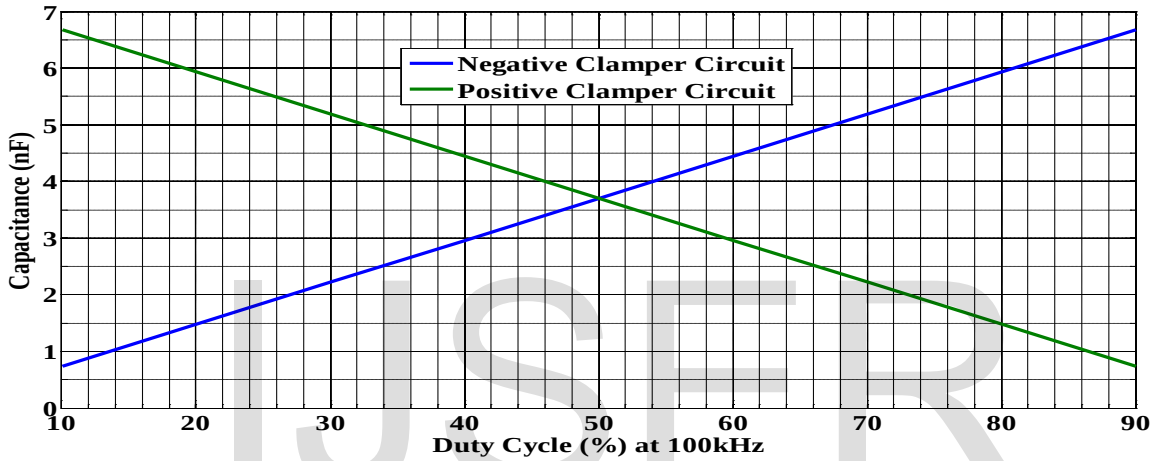

Figure 7: Effect of input voltage duty cycle on the capacitor value for positive and negative clamper circuit

In Figure 7, it was also observed that at 50% duty cycle, the capacitance values for negative and positive clamper circuits were the same.

The results in Table 2 were obtained by simulating equations (7) and (14). Table 2 showed how the resistance value (R) varied with the duty cycle for both positive and negative clamper circuits for 100kHz frequency input signal. The table showed that for negative clamper circuit, the resistance is inversely proportional to the duty cycle while for positive clamper circuit; the resistance is directly proportional to the duty cycle of the input signal.

Table 2: Effect of input voltage duty cycle on the Resistor value for positive and negative clamper circuit

Clamper Circuit Type	Input voltage duty cycle (%) at 100kHz								
	10.00	20.00	30.00	40.00	50.00	60.00	70.00	80.00	90.00
	Resistance Value (kΩ)								
Negative	2430.00	1080.00	630.00	405.00	270.00	180.00	115.71	67.50	30.00
Positive	30.00	67.50	115.71	180.00	270.00	405.00	630.00	1080.00	2430.00

The result in Table 2 was clearly presented in Figure 8. The figure also showed that resistance for negative clamper was inversely proportional while the resistance of positive clamper was directly proportional to the input signal duty cycle.

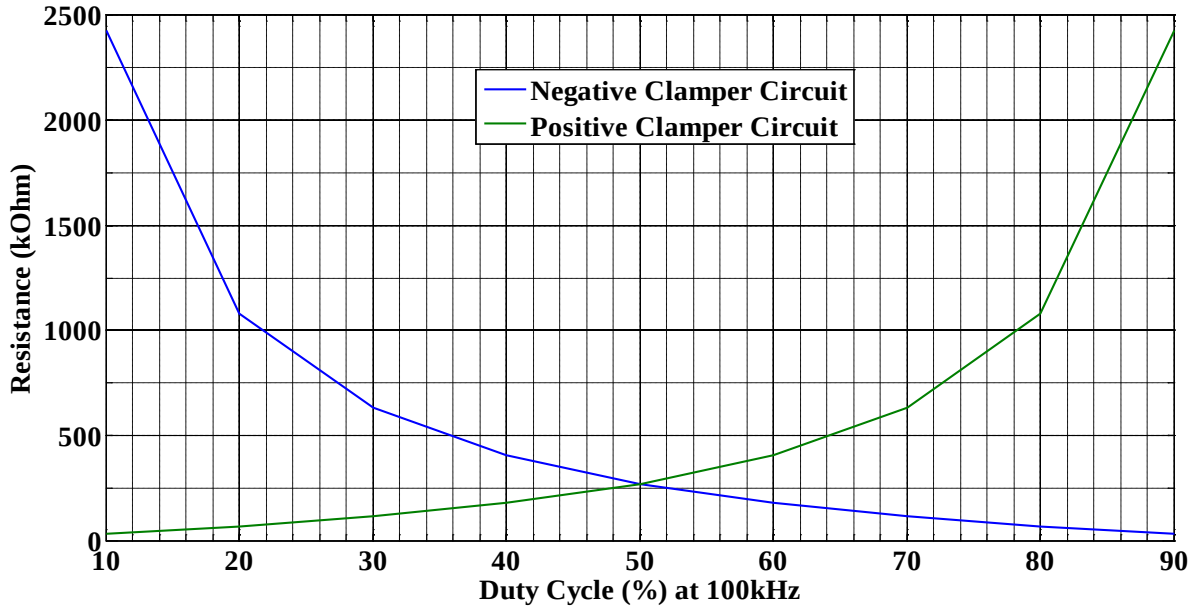

Figure 8: Effect of input voltage duty cycle on the Resistor value for positive and negative clamper circuit.

In Figure 8, it was also observed that at 50% duty cycle, the resistance value for negative and positive clamper circuits was the same. Equations (7) and (14) also showed that the resistance value was independent of the signal of the input signal.

The results in Table 3 were obtained from equations (3) and (10). Table 3 showed how the capacitance value (C) varied with the period of the input signal for both positive and negative clamper circuits for 60% duty cycle. The table showed that for both positive and negative clamper circuits, the capacitance is directly proportional to the input signal period.It also showed that negative clamper circuit requires higher capacitance value that positive clamper circuit at lower input signal frequency.

Table 3: Effect of input voltage period on the capacitor value for positive and negative clamper circuit

Clamper Circuit Type	Period (µs) at 60% duty cycle								
	10.00	21.11	32.22	43.33	54.44	65.56	76.67	87.78	98.89
	Capacitor Value (nF)								
Negative	4.44	9.38	14.32	19.26	24.20	29.14	34.07	39.01	43.95
Positive	2.96	6.26	9.55	12.84	16.13	19.42	22.72	26.01	29.30

The result in Table 3 was clearly presented in Figure 9. The figure also showed that capacitance value for both negative clamper and positive clamper was directly proportional to the period of theinput signal at 60% duty cycle.

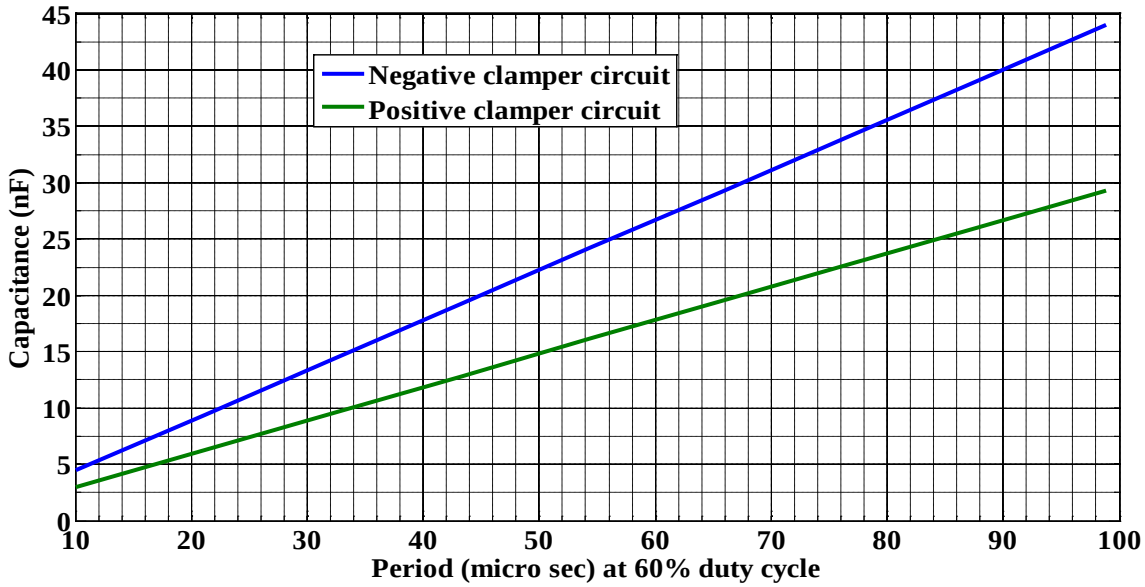

Figure 9: Effect of input voltage period on the capacitor value for positive and negative clamper circuit.

The results in Table 4 were generated from equations (1), (6), (8) and (13). Equations (1) and (2) represented the output voltages of negative clamper circuit during charging and discharging cycle respectively. On the other hand, equations (8) and (13) represented the output voltages of positive clamper circuit during charging and discharging cycle respectively. From Table 4, it was observed that for negative clamper circuit, the output voltage was 0.7V throughout the charging cycle and the output voltage fell steadily from -9.30V to -9.28V during the discharge cycle. Considering the positive clamper, the output voltage remained at -0.7V during the charging period and the output voltage fell steadily from 9.29V to 9.26V during the discharge cycle.The input signal used in the simulation was a square wave with 60% duty cycle, thefrequency of 100kHz and voltage amplitude of ±5V.

Table 4: Input and output voltage for positive and negative clamper circuits for 100 kHz frequency and 60% duty cycle input signal.

Input Signal												
Time (micro sec)	0.00	1.00	2.00	3.00	4.00	5.00	6.00	6.00	7.00	8.00	9.00	10.00
Input Voltage(V	5.00	5.00	5.00	5.00	5.00	5.00	5.00	-5.00	-5.00	-5.00	-5.00	-5.00
Negative Clamper circuit												
Time (micro sec)	0.00	1.00	2.00	3.00	4.00	5.00	6.00	6.00	7.00	8.00	9.00	10.00
Output Voltage(V)	0.70	0.70	0.70	0.70	0.70	0.70	0.70	-9.30	-9.29	-9.29	-9.28	-9.28
Positive Clamper circuit												
Time (micro sec)	0	1	2	3	4	4	5	6	7	8	9	10
Output Voltage (V)	-0.70	-0.70	-0.70	-0.70	-0.70	9.29	9.28	9.28	9.27	9.27	9.27	9.26

The results in Table 4 were plotted as shown in Figure 10. From the figure, it was observed that the negative clamper clamps the signal to the negative voltage axis while the positive clamper clamps the input signal to the positive voltage axis.

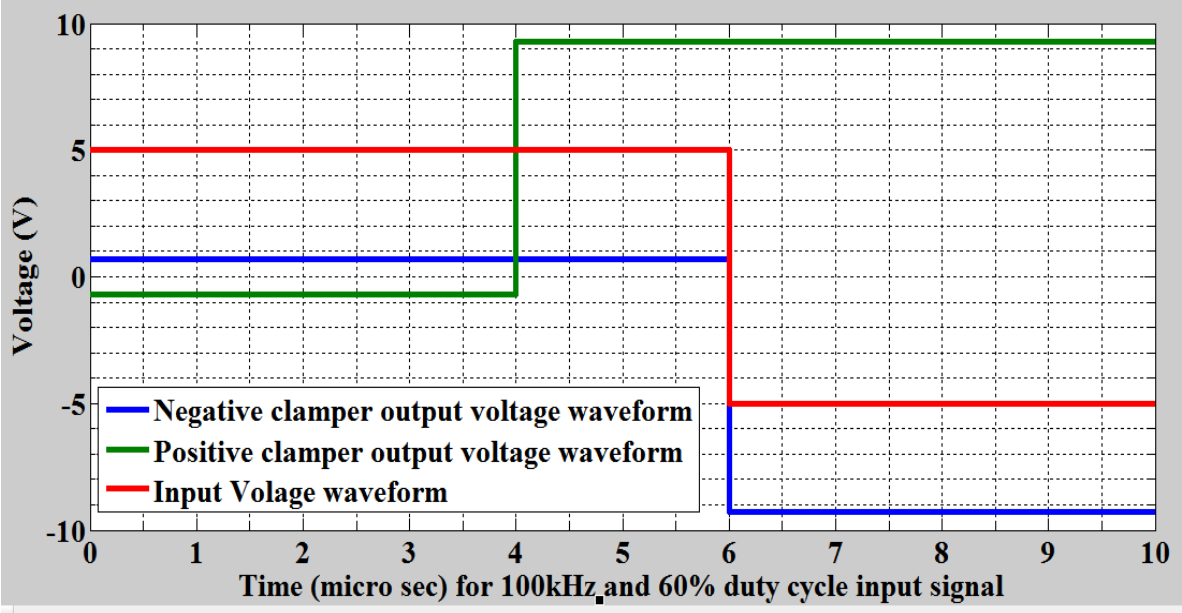

Figure 10: Plot of voltage against time for input and output signals

4.0.Model Validation Using MatLab Simscape

The models developed were validated using MatLab Simscape using 1 kHz sinusoidal input voltage. The input signal is as shown in Figure 11.The circuit diagram used in the validation of negative clamper circuit is shown in Figure 12. The voltage output from the clamper circuit in Figure 12 is shown in Figure 13. From the figure, it was observed that the output voltage has value of 0.7V during charging cycle and output of -9.3V during discharge cycle confirming what was obtained during simulation as in Figure 10.

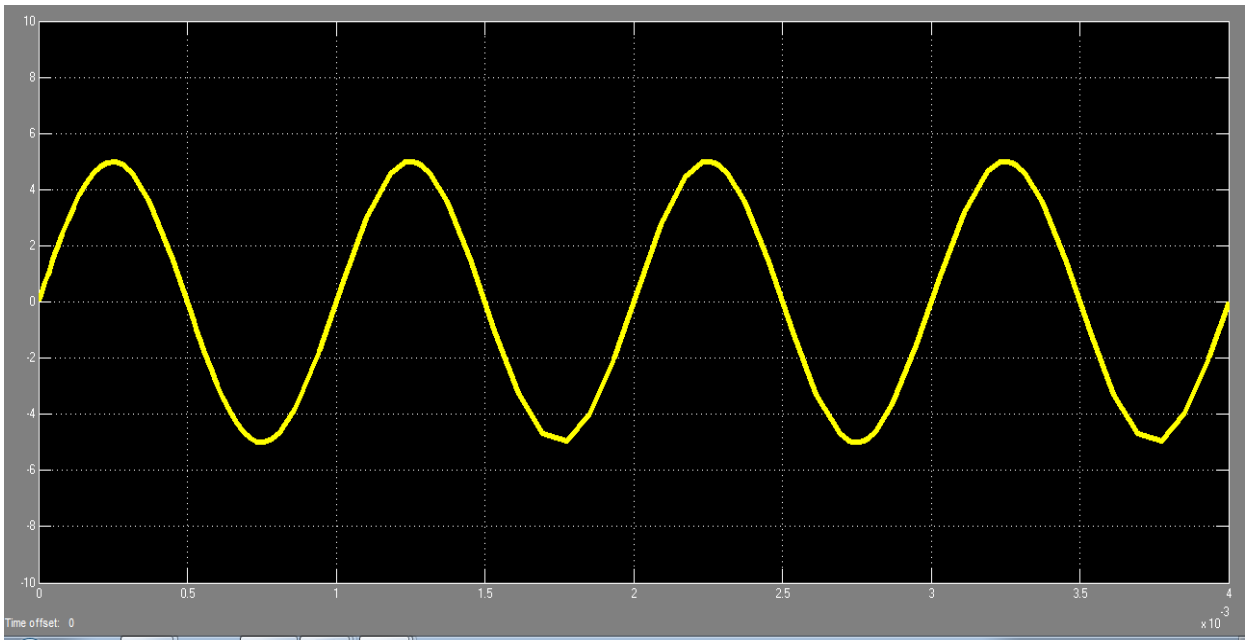

Figure 11: The input signal used in the simulations

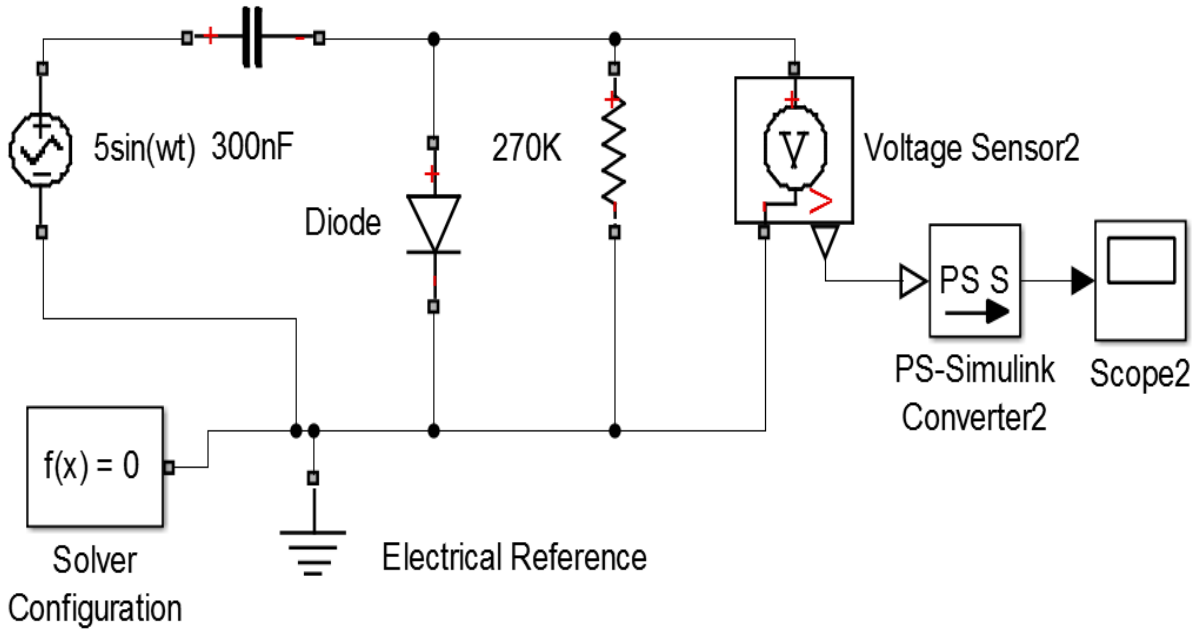

Figure 12: Negative clamper circuit using Simscape

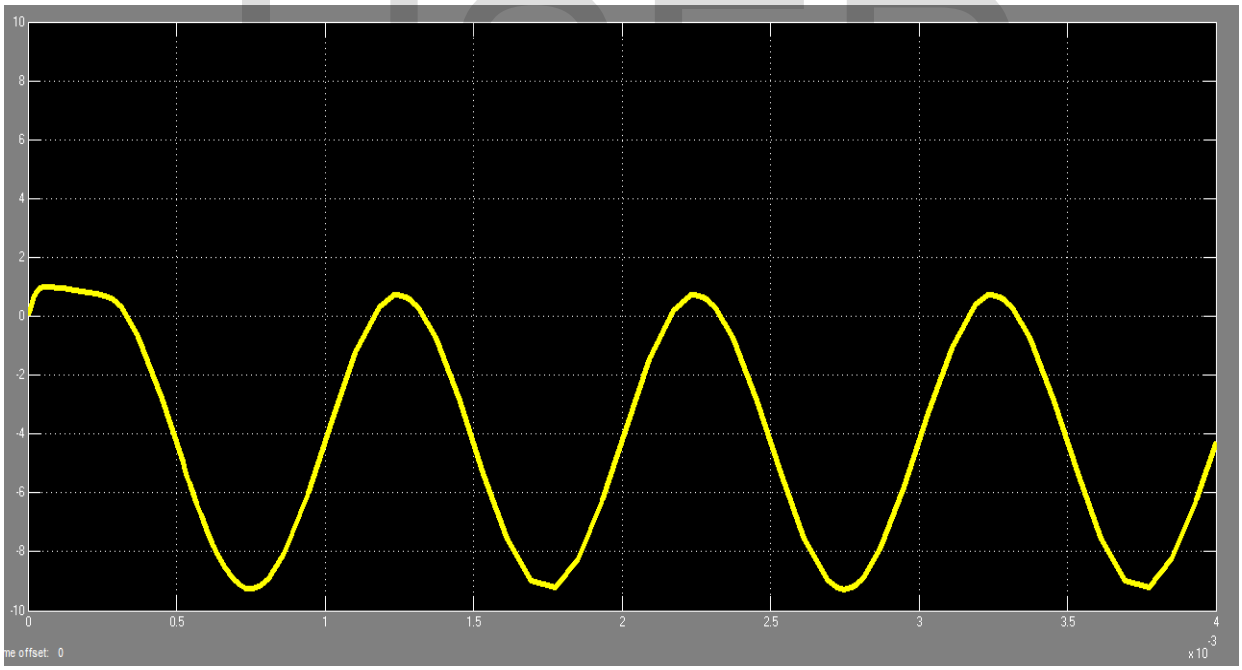

Figure 13: Output voltage of negative clamper circuit using Simscape

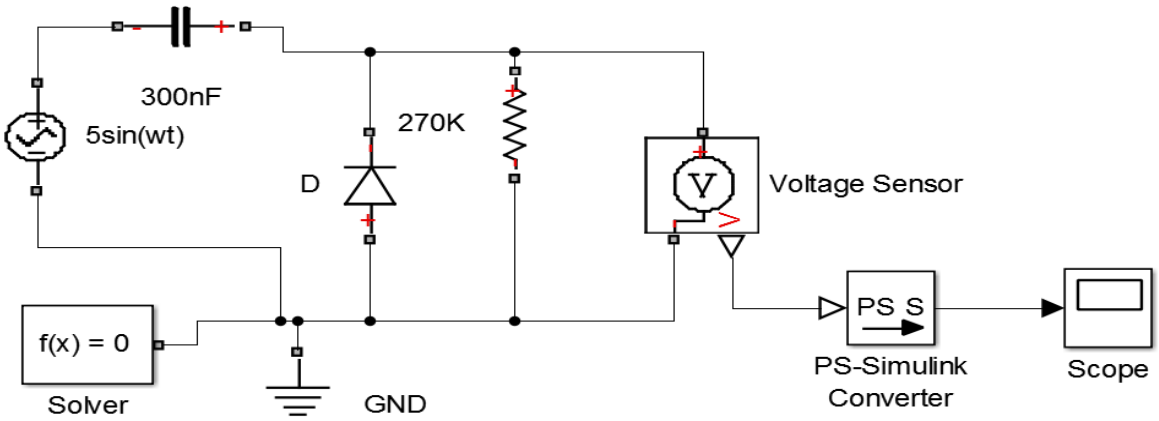

Figure 14: Positive clamper circuit using Simscape

The circuit diagram used in the validation of positive clamper circuit is shown in Figure 14. The voltage output from the clamper circuit in Figure 14 is shown in Figure 15. From the figure, it was observed that the output voltage has value of -0.7V during charging cycle and output of 9.3V during discharge cycle confirming what was obtained during simulation as in Figure 10.

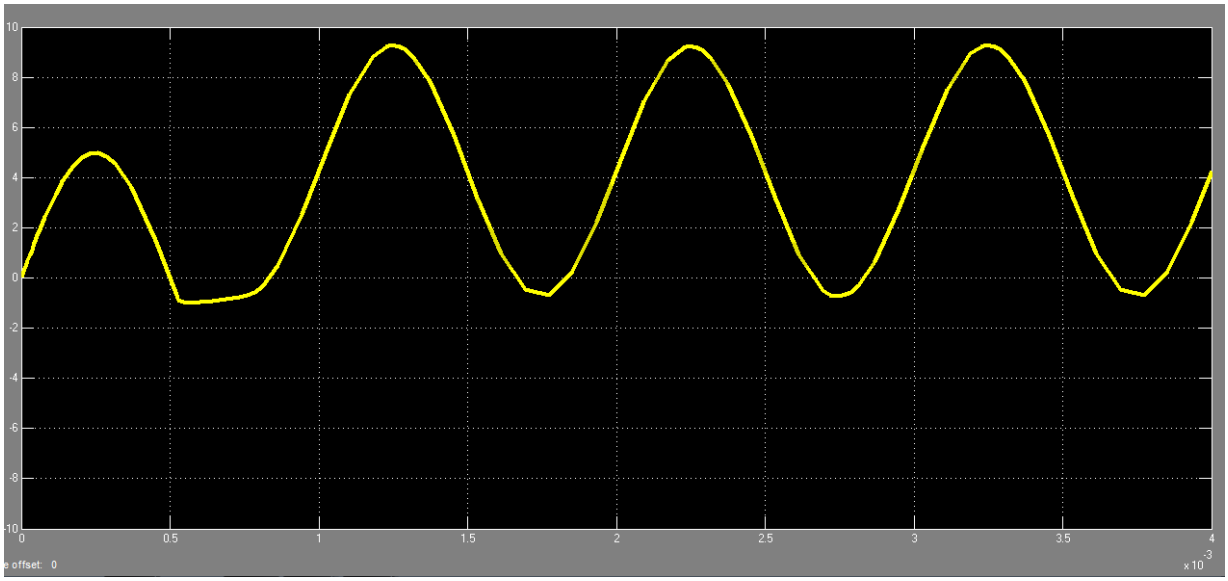

Figure 15: Output voltage of positive clamper circuit using Simscape

5.0.Conclusion

In this paper, models for passive negative and positive clamper circuits were successfully developed and simulated.From the simulation result, it was observed that the models developedreplicated what is theoretically expected.The models were also validated using Simscape and the result obtained from Simscape agreed with the result from the simulated models.The importance of this research is that it showed the new method of designing clamper circuits for electronic systems. The results obtained also acts as a lookup data for designers of clamper circuits.

Reference

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